



09/431477

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Kiran Ganesh et al.	Examiner:	Phallaka Kik
Serial No.:	09/431477	Group Art Unit:	2825
Filed:	November 1, 1999	Docket No.:	884.141US1
Title:	2-DIMENSIONAL PLACEMENT WITH RELIABILITY CONSTRAINTS FOR VLSI DESIGN		
Assignee:	Intel Corporation	Confirmation No.	8764

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**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicant has reviewed the Office Action mailed on September 25, 2003. Please amend the above-identified patent application as follows.

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a three-month extension of the period for responding to the Office action, thereby moving the deadline for response from December 25, 2003 to March 25, 2004.